AMENDMENTS TO THE CLAIMS

Please amend the claims as presented below and cancel claim 8 without prejudice or disclaimer.

1. (Previously presented) A data transferring apparatus as claimed in claim 4, wherein said decode unit further comprises:

a data transferring unit for transferring said liquid ejection data compressed to be capable of line development to said decode circuit via said system bus and transferring said developed liquid ejection data to said system bus.

2. (Original) A data transferring apparatus as claimed in claim 1, wherein said decode unit further comprises:

a line buffer for storing said liquid ejection data developed by said decode circuit by word unit, and

a DMA transferring unit for performing DMA transfer on said liquid ejection data compressed to be capable of line development to said decode circuit from said system memory, performing DMA transfer on said liquid ejection data developed in said line buffer to said system memory by word unit, and performing sequential DMA transfer on said developed liquid ejection data stored in said system memory to a register of a liquid ejecting head.

3. (Original) A data transferring apparatus as claimed in claim 2, wherein said line buffer further comprises two (2) faces of buffer areas for storing developed data of predetermined words, said liquid ejection data developed by said decode circuit is sequentially stored in a first face of said buffer areas, while said liquid ejection data developed by said decode circuit is sequentially stored in a second face of said buffer areas when said developed data of predetermined words is accumulated, and DMA

transfer to said system memory is performed per predetermined words with respect to said developed data when said developed data of predetermined words is accumulated.

4. (Previously presented) A data transferring apparatus for transferring liquid ejection data, comprising:

a system bus;

an interface unit for receiving liquid ejection controlling data which comprises liquid ejection data compressed to be capable of line development;

a receiving buffer unit comprising an interface memory for storing liquid ejection data compressed to be capable of line development;

said receiving buffer unit further comprises:

a command storing register which is accessible from said system bus,

a header analyzing unit for analyzing a header of said liquid ejection controlling data,

a command separating unit for separating a command from said liquid ejection controlling data according to said analysis result of said header analyzing unit and storing said command into said command storing register, and

a data transfer controlling unit for storing liquid ejection controlling data, from which said command is separated, into said interface memory;

a decode unit comprising a decode circuit, which can perform hardware development on liquid ejection data compressed to be capable of line development and stored in said interface memory;

said decode unit further comprises:

a line buffer for storing said liquid ejection data developed by said decode circuit by word unit, and

a DMA transferring unit for performing DMA transfer on said liquid ejection data compressed to be capable of line development to said decode

circuit from said interface memory, performing DMA transfer on said liquid ejection data developed in said line buffer to said system memory by word unit, and performing sequential DMA transfer on said developed liquid ejection data stored in said system memory to a register of a liquid ejecting head;

said line buffer further comprises two (2) faces of buffer areas for storing developed data of predetermined words, said liquid ejection data developed by said decode circuit is sequentially stored in a first face of said buffer areas, while said liquid ejection data developed by said decode circuit is sequentially stored in a second face of said buffer areas when said developed data of predetermined words is accumulated, and DMA transfer to said system memory is performed per predetermined words with respect to said developed data when said developed data of predetermined words is accumulated;

a system memory for storing said liquid ejection data developed in said decode circuit;

a head controlling unit comprising a register of a liquid ejecting head;

a first dedicated bus for coupling said interface unit to said receiving buffer unit;

a second dedicated bus for coupling said receiving buffer unit to said decode unit; and

a third dedicated bus for coupling said decode unit to said head controlling unit,

wherein said interface unit, said receiving buffer unit, said decode unit and said system memory are coupled to said system bus in order to be able to transfer data.

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Cancelled)

9. (Currently amended) A data transferring apparatus as claimed in claim ~~7~~ 4, wherein

said receiving buffer unit further comprises a data separating unit for separating said liquid ejection controlling data stored in said interface memory into a remote command and liquid ejection data compressed to be capable of line development,

said remote command is processed by a microprocessor coupled to said system bus, and

said liquid ejection data compressed to be capable of line development is transferred to said decode unit.

10. (Previously presented) A data transferring apparatus ~~as claimed in claim 4,~~ for transferring liquid ejection data, comprising:

a system bus;

an interface unit for receiving liquid ejection controlling data which comprises liquid ejection data compressed to be capable of line development;

a decode unit comprising a decode circuit, which can perform hardware development on liquid ejection data compressed to be capable of line development and stored in said interface memory;

a receiving buffer unit comprising an interface memory for storing liquid ejection data compressed to be capable of line development;

wherein said receiving buffer unit further comprises:

a data transfer controlling unit for storing liquid ejection controlling data received by said interface unit into said interface memory, and

a data separating unit for separating said liquid ejection controlling data stored in said interface memory into a command and liquid ejection data compressed to be capable of line development,

wherein said command is processed by a microprocessor coupled to said system bus, and

said liquid ejection data compressed to be capable of line development is transferred to said decode unit;

a system memory for storing said liquid ejection data developed in said decode circuit;

a head controlling unit comprising a register of a liquid ejecting head;

a first dedicated bus for coupling said interface unit to said receiving buffer unit;

a second dedicated bus for coupling said receiving buffer unit to said decode unit; and

a third dedicated bus for coupling said decode unit to said head controlling unit,

wherein said interface unit, said receiving buffer unit, said decode unit and said system memory are coupled to said system bus in order to be able to transfer data.

11. (Original) A data transferring apparatus as claimed in claim 4, wherein one (1) ASIC comprises said interface unit, said receiving buffer unit, said decode unit, said head controlling unit and said first, second and third dedicated buses.

12. (Original) A data transferring apparatus as claimed in claim 1, wherein said compressed liquid ejection data is run length compression data, and said decode circuit can perform hardware development on run length compression data.

13. (Currently amended) A liquid ejecting apparatus comprising a data transferring apparatus as claimed in one of claims 1 – 4, ~~to~~ 9 – 12, or 14 – 18.

14. (New) A data transferring apparatus as claimed in claim 10, wherein said decode unit further comprises:

a data transferring unit for transferring said liquid ejection data compressed to be capable of line development to said decode circuit via said system bus and transferring said developed liquid ejection data to said system bus.

15. (New) A data transferring apparatus as claimed in claim 14, wherein said decode unit further comprises:

a line buffer for storing said liquid ejection data developed by said decode circuit by word unit, and

a DMA transferring unit for performing DMA transfer on said liquid ejection data compressed to be capable of line development to said decode circuit from said system memory, performing DMA transfer on said liquid ejection data developed in said line buffer to said system memory by word unit, and performing sequential DMA transfer on said developed liquid ejection data stored in said system memory to a register of a liquid ejecting head.

16. (New) A data transferring apparatus as claimed in claim 15, wherein said line buffer further comprises two (2) faces of buffer areas for storing developed data of predetermined words, said liquid ejection data developed by said decode circuit is sequentially stored in a first face of said buffer areas, while said liquid ejection data developed by said decode circuit is sequentially stored in a second face of said buffer areas when said developed data of predetermined words is accumulated, and DMA transfer to said system memory is performed per predetermined words with respect to said developed data when said developed data of predetermined words is accumulated.

17. (New) A data transferring apparatus as claimed in claim 10, wherein one (1) ASIC comprises said interface unit, said receiving buffer unit, said decode unit, said head controlling unit and said first, second and third dedicated buses.

18. (New) A data transferring apparatus as claimed in claim 14, wherein said compressed liquid ejection data is run length compression data, and said decode circuit can perform hardware development on run length compression data.